

PROTECTION PRODUCTS

Description

RailClamp® TVS arrays are low capacitance ESD protection devices designed to protect sensitive components from overvoltage caused by electrostatic discharge (ESD), electrical fast transients (EFT), and lightning surge. It offers desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

The unique design incorporates surge rated, low capacitance steering diodes and a TVS diode in a single package. During transient conditions, the steering diodes direct the transient current to ground via the internal low voltage TVS. The TVS diode clamps the transient voltage to a safe level. The low capacitance array configuration allows the user to protect up to four data lines.

The SRDA3.3-4 is constructed using Semtech's proprietary EPD process technology. The EPD process provides low stand-off voltages with significant reductions in leakage current and capacitance over silicon avalanche diode processes. They feature a true operating voltage of 3.3 volts for superior protection. These devices are in a 8-pin SOIC package. It measures 3.9 x 4.9mm. The high surge capability ($I_{pp}=25A$, $t_p=8/20\mu s$) means it can be used in high threat environments in applications such as CO/CPE equipment, telecommunication lines, and video lines.

Features

- Transient protection for high-speed data lines to
 - ♦ IEC 61000-4-2 (ESD) $\pm 15kV$ (air), $\pm 8kV$ (contact)
 - ♦ IEC 61000-4-4 (EFT) 40A (5/50ns)
 - ♦ IEC 61000-4-5 (Lightning) 25A (8/20 μs)
- Array of surge rated diodes with internal TVS diode
- Protects four I/O lines
- Low capacitance (<15pF)
- Low operating voltage: 3.3V
- Low clamping voltage
- Solid-state technology

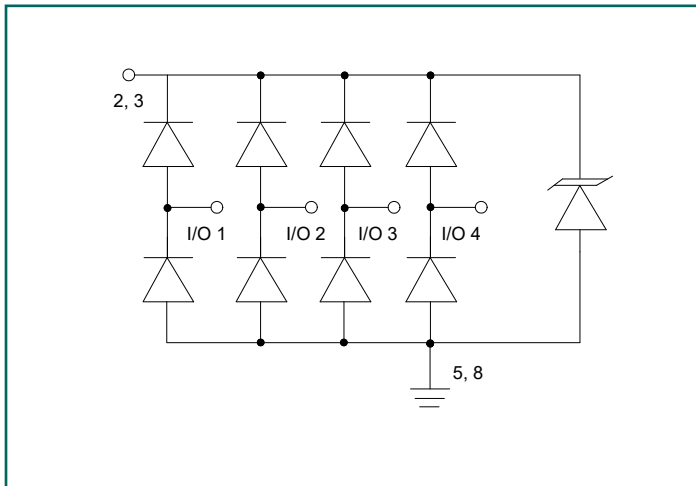
Mechanical Characteristics

- JEDEC SOIC-8 Package
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Lead Finish: Matte Sn
- Marking : Marking Code
- Packaging : Tape and Reel

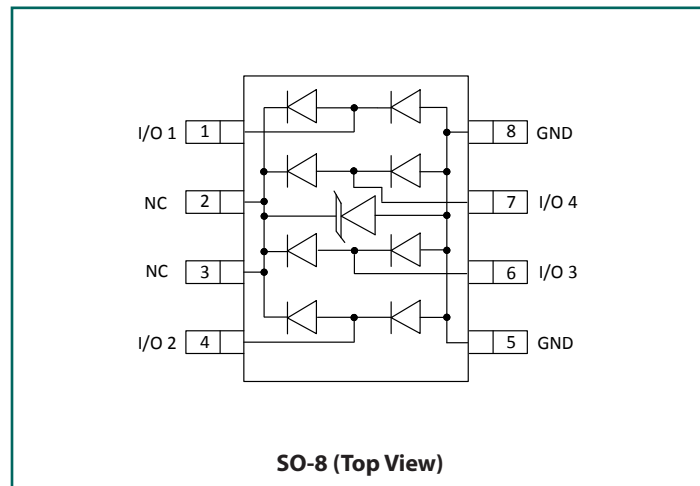
Applications

- T1/E1 secondary IC Side Protection
- T3/E3 secondary IC Side Protection
- Analog Video Protection
- Microcontroller Input Protection
- Base stations
- I²C Bus Protection

Circuit Diagram



Schematic and Pin Configuration



Absolute Maximum Ratings

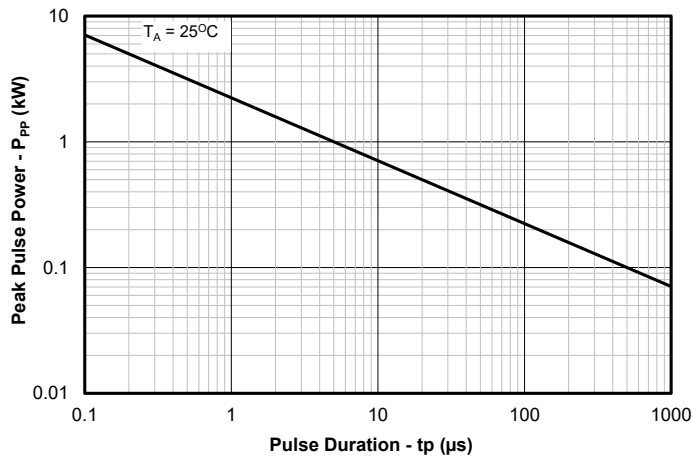
Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P _{PK}	500	W
Peak Pulse Current (tp = 8/20μs)	I _{PP}	25	A
Lead Soldering Temperature	T _L	260 (10 sec.)	°C
Operating Temperature	T _{OP}	-40 to +85	°C
Storage Temperature	T _{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C unless otherwise specified)

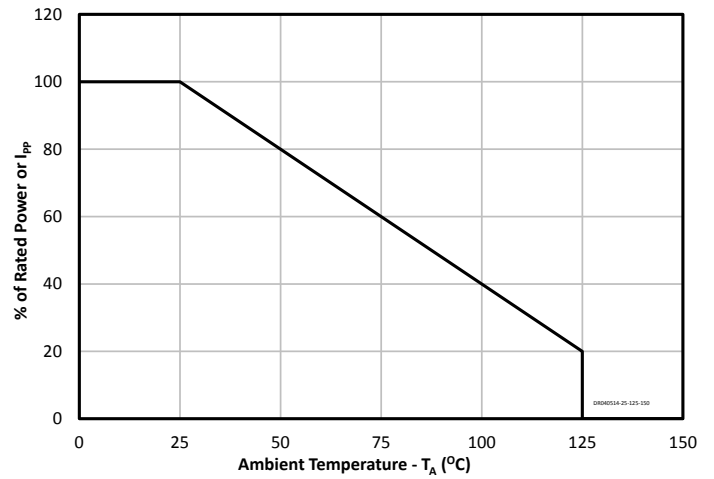
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V _{RWM}				3.3	V
Punch-Through Voltage	V _{PT}	I _{PT} = 2μA	3.5			V
Snap-Back Voltage	V _{SB}	I _{SB} = 50mA	2.8			V
Reverse Leakage Current	I _R	V _{RWM} = 3.3V			1	μA
Clamping Voltage	V _C	tp = 8/20μs	I _{PP} = 1A		5.3	V
			I _{PP} = 10A		10	
			I _{PP} = 25A		15	
Junction Capacitance	C _J	V _R = 0V, f = 1MHz	I/O to GND	8	15	pF
			I/O to I/O	4		

Typical Characteristics

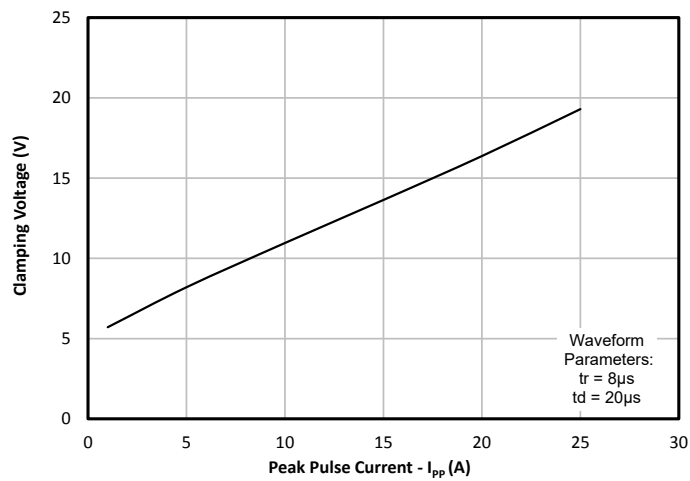
Non-Repetitive Peak Pulse Power vs. Pulse Time



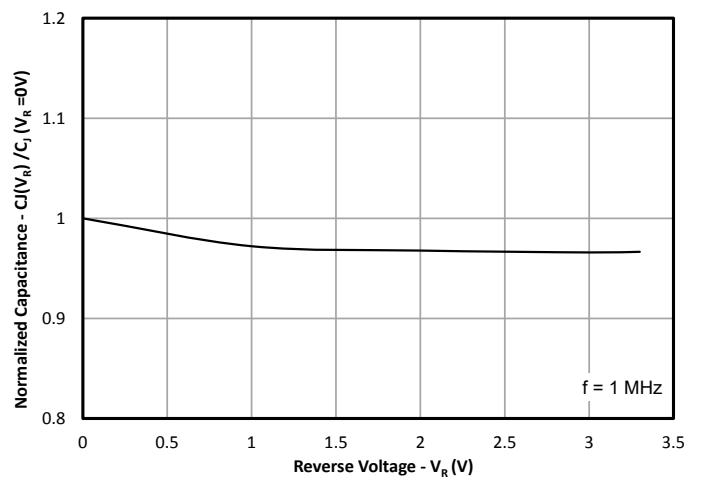
Power Derating Curve



Clamping Voltage vs. Peak Pulse Current



Normalized Junction Capacitance vs. Reverse Voltage



Application Information

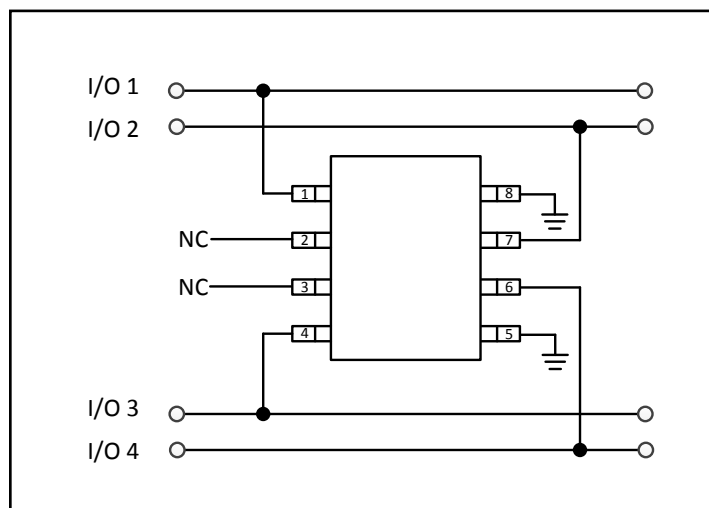
Device Connection Options for Protection of Four High-Speed Data Lines

These devices are designed to protect low voltage data lines operating at 3.3 V. When the voltage on the protected line exceeds the punch-through or “turn-on” voltage of the TVS diode, the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry.

Data lines are connected at pins 1, 4, 6 and 7. Pins 5 and 8 should be connected directly to a ground plane. The path length is kept as short as possible to minimize parasitic inductance.

Note that pins 2 and 3 are connected internally to the cathode of the low voltage TVS. It is not recommended that these pins be directly connected to a DC source greater than the snap-back voltage (V_{SB}) as the device can latch on as described below.

Data Line Protection Using Internal TVS Diode as Reference



EPD TVS IV Characteristic Curve

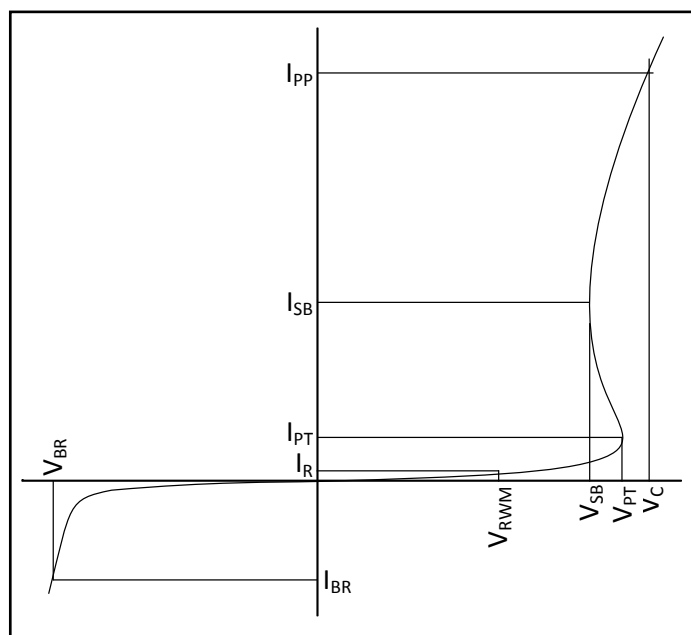
These devices are constructed using Semtech’s proprietary EPD technology. By utilizing the EPD technology, the SRDA3.3-4 can effectively operate at 3.3V while maintaining excellent electrical characteristics.

The EPD TVS employs a complex npn structure in contrast to the pn structure normally found in traditional silicon-avalanche TVS diodes. Since the EPD TVS devices use a 4-layer structure, they exhibit a slightly different IV

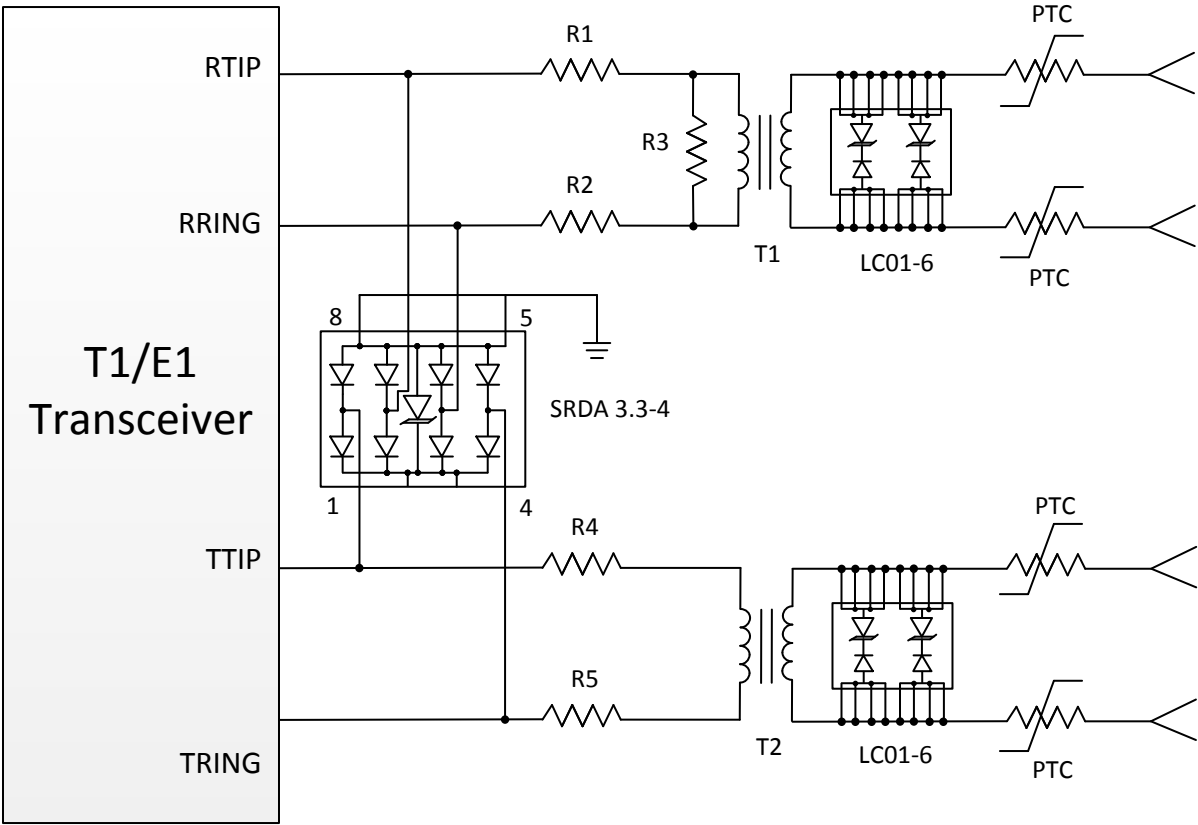
characteristic curve when compared to conventional devices. During normal operation, the device represents a high-impedance to the circuit up to the device working voltage (V_{RWM}). During an ESD event, the device will begin to conduct and will enter a low impedance state when the punch through voltage (V_{PT}) is exceeded. Unlike a conventional device, the low voltage TVS will exhibit a slight negative resistance characteristic as it conducts current. This characteristic aids in lowering the clamping voltage of the device, but must be considered in applications where DC voltages are present.

When the TVS is conducting current, it will exhibit a slight “snap-back” or negative resistance characteristics due to its structure. This point is defined on the curve by the snap-back voltage (V_{SB}) and snap-back current (I_{SB}). To return to a non-conducting state, the current through the device must fall below the I_{SB} (approximately $<50mA$) and the voltage must fall below the V_{SB} (normally 2.8V for a 3.3 V device). If a 3.3 V TVS is connected to 3.3V DC source, it will never fall below the snap-back voltage of 2.8V and will therefore stay in a conducting state.

EPD TVS IV Characteristic Curve

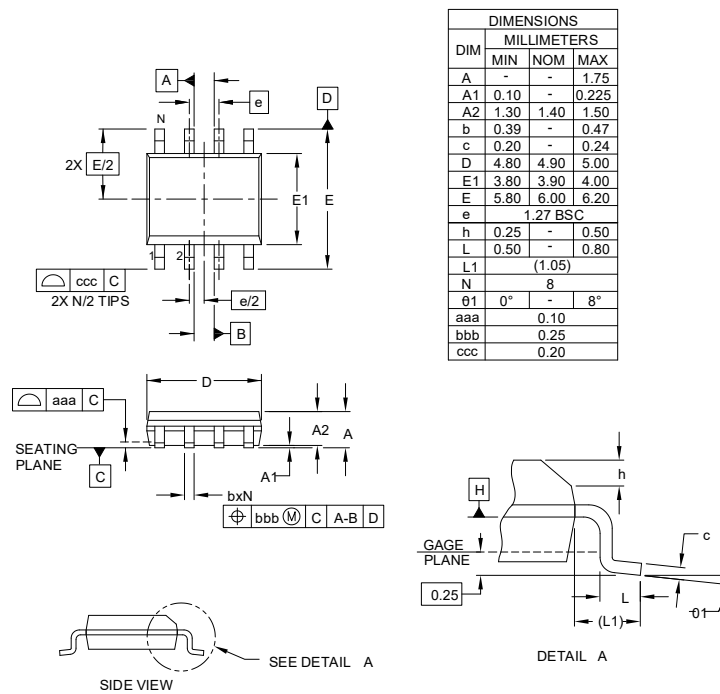


Typical Application



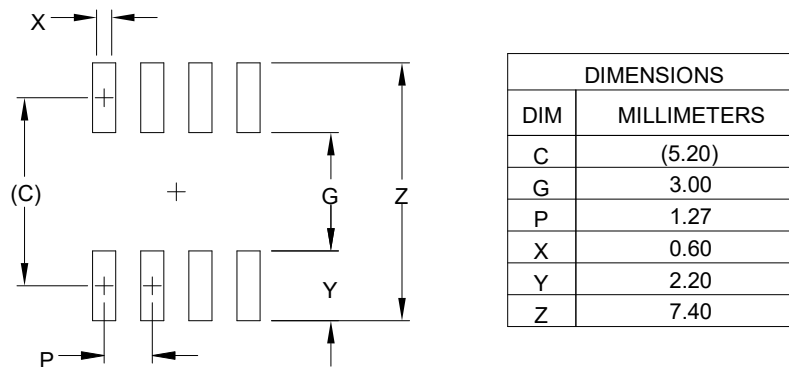
T1/E1 Interface Protection (GR-1089 Long Haul)

Outline Drawing - SO-8



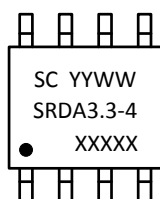
- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
 2. DATUMS $\boxed{-A-}$ AND $\boxed{-B-}$ TO BE DETERMINED AT DATUM PLANE $\boxed{-H-}$.
 3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
 4. REFERENCE JEDEC STD MS-012, VARIATION AA.

Land Pattern - SO-8



- NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
 2. REFERENCE IPC-SM-782A, RLP NO. 300A.

Marking Code

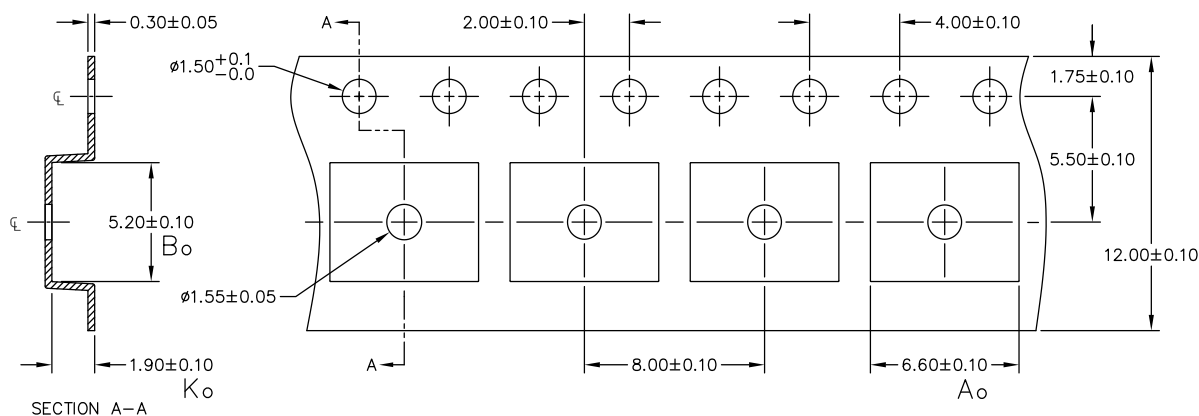


Notes:

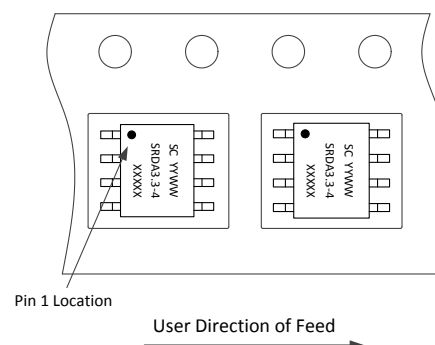
YYWW = Date Code

XXXXX = Country of Assembly

Tape and Reel Specification



NOTE: ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.



Ordering Information

Part Number	Lead Finish	Qty per Reel	Reel Size
SRDA3.3-4.TLT	Matte Sn	3000	13 Inch



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